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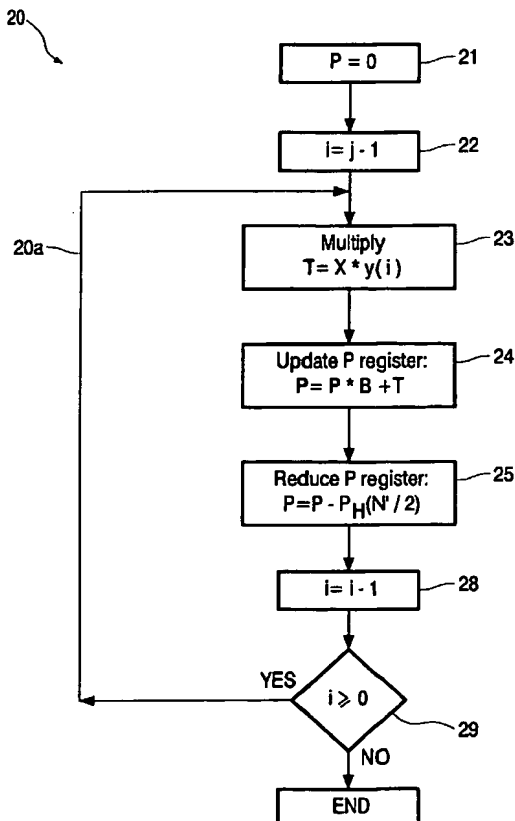
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[Continued on next page]

(54) Title: **QUISQUATER REDUCTION**



(57) Abstract: A method and apparatus for calculating the product P of a first number X and a second number Y, modulo N, where Y is partitioned into j words each of length p bits, and has a length (m + n) bits, cyclically operates on successive ones of the j words of Y, carrying out intermediate modulo reductions of the intermediate products formed. A specially selected multiple, N', of N is used so that only a single reduction of the intermediate product P is never longer than (m+n) bits at the end of each cycle. N' is an integer multiple of N, and the value N' is selected such that the (m - 1) most significant bits are equal to '1', and the least significant bit is '0'.



SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 366 673 B1 (VAN DIJK MARTEN E ET AL) 2 April 2002 (2002-04-02) abstract column 3, line 1 - column 6, line 9 -----	1-15
A	ORTON G ET AL: "A DESIGN OF A FAST PIPELINED MODULAR MULTIPLIER BASED ON A DIMINISHED-RADIX ALGORITHM" JOURNAL OF CRYPTOLOGY, NEW YORK, NY, US, vol. 5, 1992, pages 183-208, XP000669945 abstract figures 1,4 -----	1-15
A	DE 101 42 155 C (INFINEON TECHNOLOGIES AG) 23 May 2002 (2002-05-23) abstract page 6, line 59 - page 7, line 37 page 8, line 15 - page 9, line 52 figures 4-7 -----	1-15

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